IN THE CLAIMS:

Claims 1 through 25 and 39 were previously cancelled. None of the claims have been amended herein. All of the pending claims are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as previously amended.

1.-25. (Cancelled)

26. (Previously presented) A semiconductor substrate assembly, comprising:

at least one semiconductor die having a plurality of bond pads formed on an active surface thereof;

at least one anisotropically conductive layer comprising a plurality of laterally isolated conductive elements disposed in a dielectric material and having upper ends exposed therethrough attached to the active surface;

a plurality of conductive bumps on the at least one anisotropically conductive layer with each conductive bump in contact with at least one conductive element of the plurality; and

wire bonds extending between the bond pads and the conductive bumps.

27. (Original) The assembly of claim 26, wherein the at least one anisotropically conductive layer comprises conductive elements in the form of discrete metal columns embedded in a polymeric material.

28. (Original) The assembly of claim 27, wherein the discrete metal columns have a diameter of about 1 μm to about 15 μm.

29. (Original) The assembly of claim 27, wherein the discrete metal columns have a diameter of about 2 μm to about 8 μm.

30. (Original) The assembly of claim 27, wherein the polymeric material comprises a tape or film.

31. (Original) The assembly of claim 26, wherein the conductive elements comprise at least one of tungsten, aluminum, copper, silver, gold, and alloys thereof.

32. (Original) The assembly of claim 26, wherein the at least one anisotropically conductive layer is attached to the active surface by an adhesive.

33. (Previously presented) The assembly of claim 26, further comprising:
a substrate having a plurality of terminal pads on a surface thereof; and
wire bonds extending between the plurality of conductive bumps and the plurality of terminal pads.

34. (Original) The assembly of claim 33, wherein the substrate comprises one of a circuit board, an interposer, a semiconductor die, a wafer and a partial wafer.

35. (Original) The assembly of claim 32, further comprising a dielectric layer over the at least one semiconductor die, the bond pads, the conductive bumps and the wire bonds.

36. (Original) The assembly of claim 26, wherein the conductive bumps are attached to the conductive elements by metallurgical bonds.

37. (Original) The assembly of claim 26, wherein the conductive bumps and the wire bonds are formed of gold.

38. (Previously presented) A semiconductor substrate assembly, comprising:

at least one semiconductor die having a plurality of bond pads formed on an active surface thereof;

at least one anisotropically conductive layer comprising a plurality of laterally isolated conductive elements disposed in a dielectric material and having upper ends exposed therethrough attached to the active surface; and

a plurality of conductive bumps on the at least one anisotropically conductive layer with each conductive bump in contact with at least one conductive element of the plurality;

wire bonds between the bond pads and the conductive bumps;

wherein the at least one semiconductor die has the plurality of bond pads centrally located along an axis thereof and the at least one anisotropically conductive layer comprises a plurality of anisotropically conductive layers adjacent the plurality of bond pads on opposing sides thereof; and

wherein the at least one semiconductor die comprises a wafer including a plurality of semiconductor dice, and the plurality of anisotropically conductive layers are disposed between pluralities of bond pads of adjacent semiconductor dice and extending over boundaries therebetween.

39. (Cancelled)

40. (Original) The assembly of claim 26, wherein the at least one semiconductor die is in the form of a singulated die, a partial wafer comprising a plurality of semiconductor dice or a wafer comprising a plurality of semiconductor dice.

41. (Previously presented) A semiconductor substrate assembly, comprising:
at least one semiconductor die having a plurality of bond pads formed on an active surface thereof;
at least one anisotropically conductive layer comprising a plurality of laterally isolated conductive elements disposed in a dielectric material and having upper ends exposed therethrough attached to the active surface;
a plurality of conductive bumps on the at least one anisotropically conductive layer with each conductive bump in contact with at least one conductive element of the plurality;
wire bonds between the bond pads and the conductive bumps; and
another plurality of conductive bumps, each conductive bump of the another plurality disposed on one of the plurality of conductive bumps.

42. (Original) The assembly of claim 41, further comprising:
a substrate having a plurality of terminal pads on a surface thereof with the conductive bumps of the another plurality in alignment with and bonded to the terminal pads.

43. (Original) The assembly of claim 42, wherein the substrate comprises one of a circuit board, an interposer, a semiconductor die, a wafer and a partial wafer.

44. (Original) The assembly of claim 43, wherein the at least one semiconductor die comprises a wafer including a plurality of semiconductor dice and the substrate comprises a wafer-scale substrate.

45. (Original) The assembly of claim 42, further comprising a dielectric underfill material between the at least one semiconductor die and the substrate.

46. (Original) The assembly of claim 41, further comprising a dielectric material covering the plurality of conductive bumps, the bond pads and the wire bonds therebetween and leaving at least a portion of each of the conductive bumps of the another plurality exposed therethrough.